The number of full and half adders are required to add 16-bit number is _____

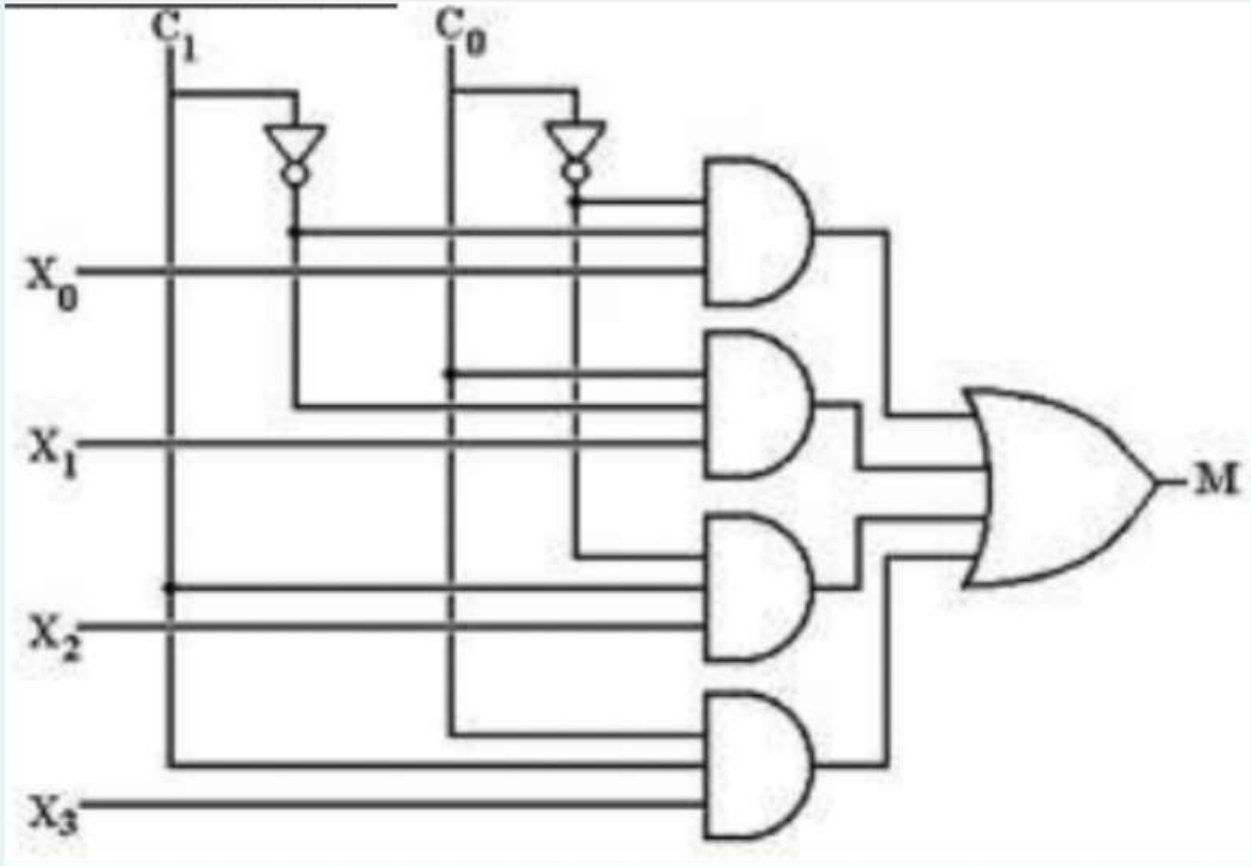
a. 16 half adders, 0 full adders

b. 4 half adders, 12 full adders

c. 1 half adders, 15 full adders

d. 8 half adders, 8 full adders

In the given 4-to-1 multiplexer, if c1 = 0 and c0 = 1 then the output M is



a. X0 OR X3

b. X1

c. X3

d. X0

e. X2

The binary numbers A = 1100 and B = 1001 are applied to the inputs of a comparator. What are the output levels?

a. $A > B = 1, A < B = 0, A < B = 1$

b. None

c. $A > B = 1, A < B = 0, A = B = 0$

d. $A > B = 0, A < B = 1, A = B = 0$

e. $A > B = 0, A < B = 1, A = B = 1$

If two inputs are active on a high priority encoder, which will be coded on the output?

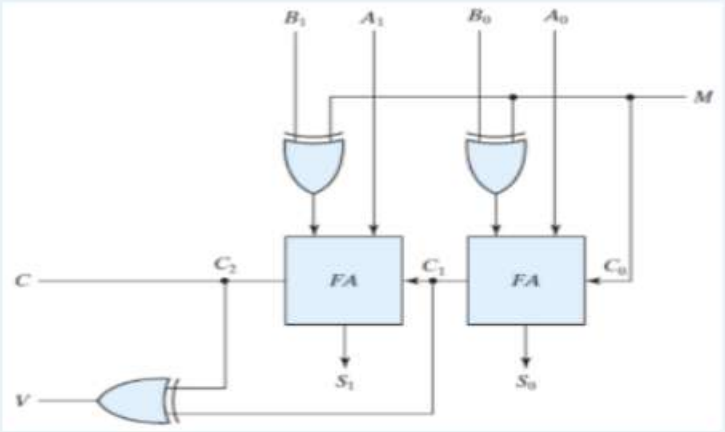
a. The higher value

b. The lower value

c. Both of the inputs

d. Neither of the inputs

For the following two-bit adder/subtractor with overflow detection. If inputs **M=0**, two unsigned numbers **A1A0= 01**, **B1B0= 01**, what's the value of **S1**, **S0**, **C**, and **V**?



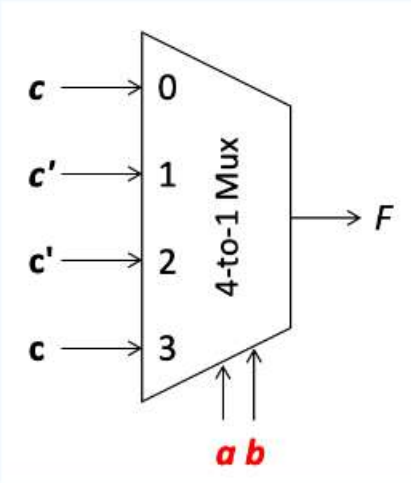
- a. **S1 S0** = 10, **C**= 1, **V**= 0
- b. **S1 S0** = 10, **C**= 1, **V**= 1
- c. **S1 S0** = 01, **C**= 1, **V**= 0
- d. **S1 S0** = 11, **C**= 1, **V**= 0
- e. **S1 S0** = 10, **C**= 0, **V**= 0

C=0

The difference between the full adder and half adder is

- a. Half adder has two inputs while full adder has four inputs
- b. Half adder has no input while full adder has three inputs
- c. Half adder has two inputs while full adder has three inputs
- d. Half adder has one input while full adder has two inputs

The following 4 x 1 multiplexer implements the function F that has an expression



a. F(a, b, c) = ∑(0, 3, 5, 6)

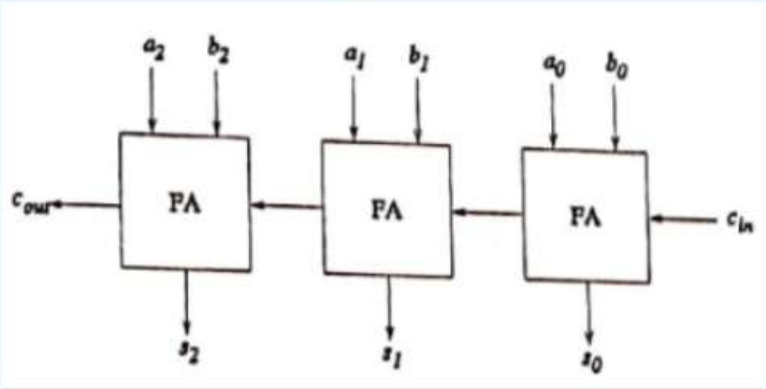
b. F(a, b, c) = ∑(1, 2, 4, 7)

c. F(a, b, c) = Π(0, 1, 3, 5, 6)

d. F(a, b, c) = ∑(1, 2, 4, 6)

e. F(a, b, c) = Π(1, 2, 4, 7)

Consider the following diagram of a 3-bit adder:



What is the value of s2, s1, s0 and Cout, if a2a1a0 = 101 and b2b1b0= 110 and Cin =0 ?

Select one:

- a. s2 s1s0 = 011 and Cout= 1
- b. s2 s1s0 = 010 and Cout= 1
- c. s2 s1s0 = 0110 and Cout= 1
- d. s2 s1s0 = 001 and Cout= 1
- e. s2 s1s0 = 011 and Cout= 0

The following switching functions are to be implemented using a decoder: f1 = ∑m(1, 2, 4, 8, 10, 14) f2 = ∑m(2, 5, 9, 11) f3 = ∑m(2, 4, 5, 6, 7) The minimum configuration of decoder will be _____

- a. 5 to 32 line
- b. 2 to 4 line
- c. 3 to 8 line
- d. 4 to 16 line

Half adder circuit can be produced using a two-input _____ gate and a two-input _____ gate.

- a. NOR; NAND
- b. OR; NAND
- c. None
- d. XOR; AND
- e. OR, AND